SEMICONDUCTOR ARRANGEMENT WITH COVERED ISLAND AND CONTACT REGIONS

Publication number: JP2004505453 (T)
Publication date: 2004-02-19
Inventor(s):
Applicant(s):
Classification:
- international: ***H01L21/337; H01L29/12; H01L29/78; H01L29/80; H01L29/808; H01L29/812; H01L29/861;*** *H01L29/24;* **H01L21/02; H01L29/02; H01L29/66;** (IPC1-7): H01L21/337; H01L29/78; H01L29/80; H01L29/808
- European: H01L29/78B2; H01L29/808B; H01L29/812B; H01L29/861
Application number: JP20020514800T 20010713
Priority number(s): DE20001036208 20000725; WO2001DE02640 20010713

Also published as:
JP4210110 (B2)
WO0209195 (A1)
US2003137010 (A1)
US6693322 (B2)
EP1303883 (A1)

Abstract not available for JP 2004505453 (T)
Abstract of corresponding document: **WO 0209195 (A1)**

The invention relates to a semiconductor arrangement for current control, comprising an n-type first semiconductor region (2) with a first surface (20), a p-type covered island region (3), within the first semiconductor region (2), with a second surface (80), an n-type contact region (5) arranged on the second surface (80) within the island region (3) and a lateral channel region (22), formed between the first and second surface (20 and 80) as part of the first semiconductor region (2). Said channel region is part of a current path from or to the contact region (5). The current (I) within the lateral channel region (22) may be influenced by at least one depleted zone (23, 24). A lateral edge (221) of the lateral channel region (22) extends as far as the contact region (5).